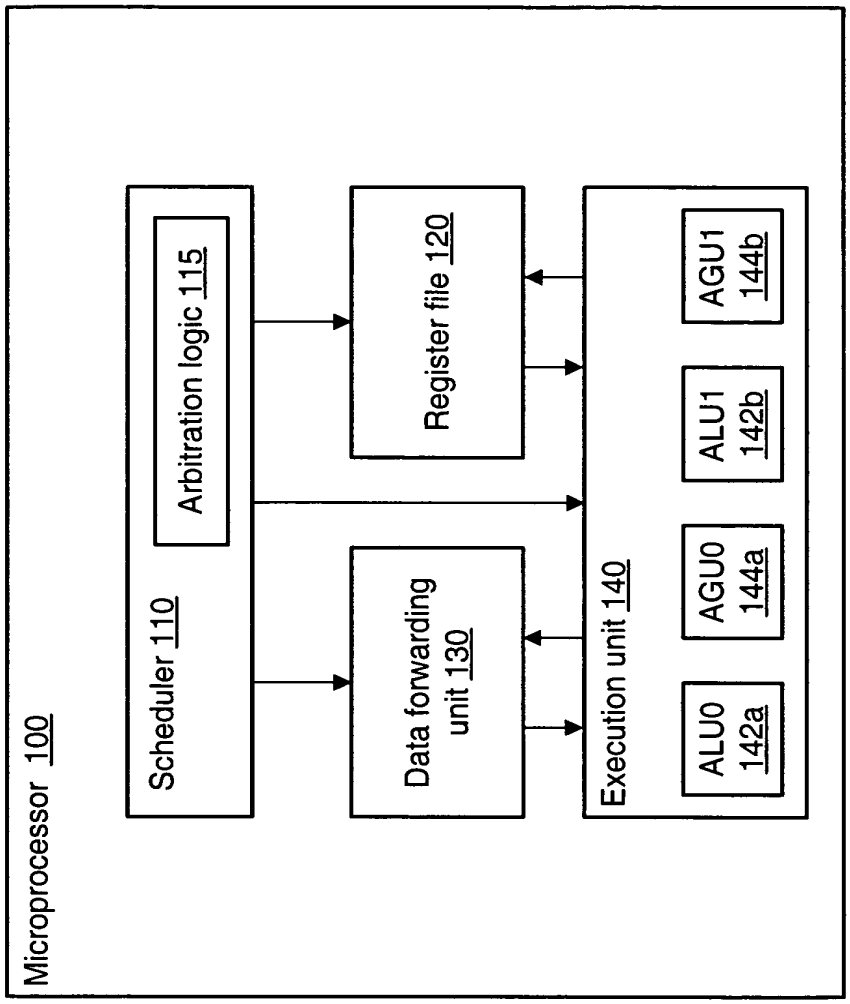
Microprocessor 100
Scheduler 110
Arbitration logic 115
Register file 120
Data forwarding unit 130
Execution unit 140
ALU0 142a
AGU0 144a
ALU1 142b
AGU1 144b

FIG. 1

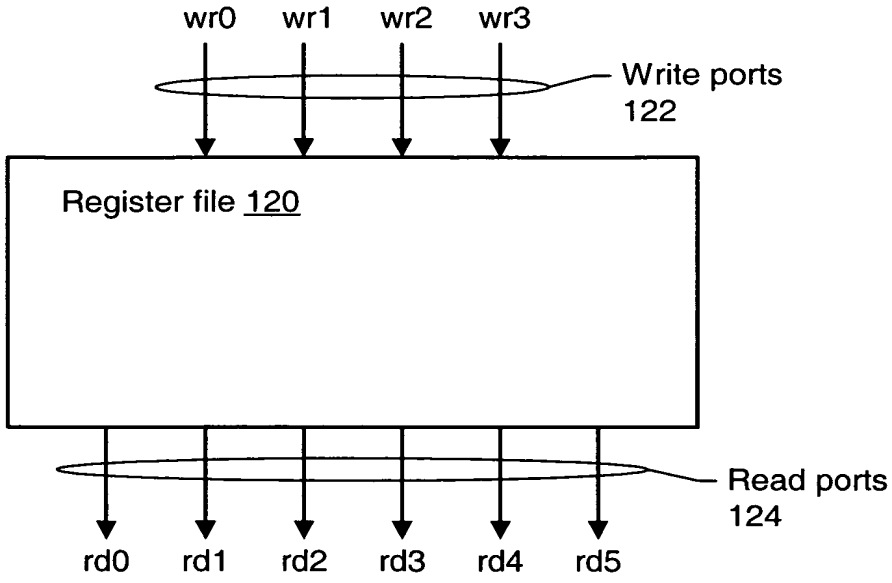

FIG. 2

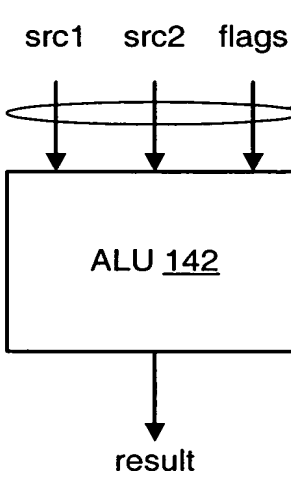

FIG. 3

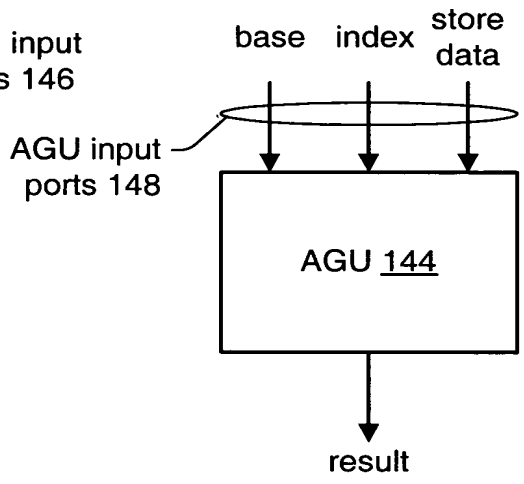

FIG. 4

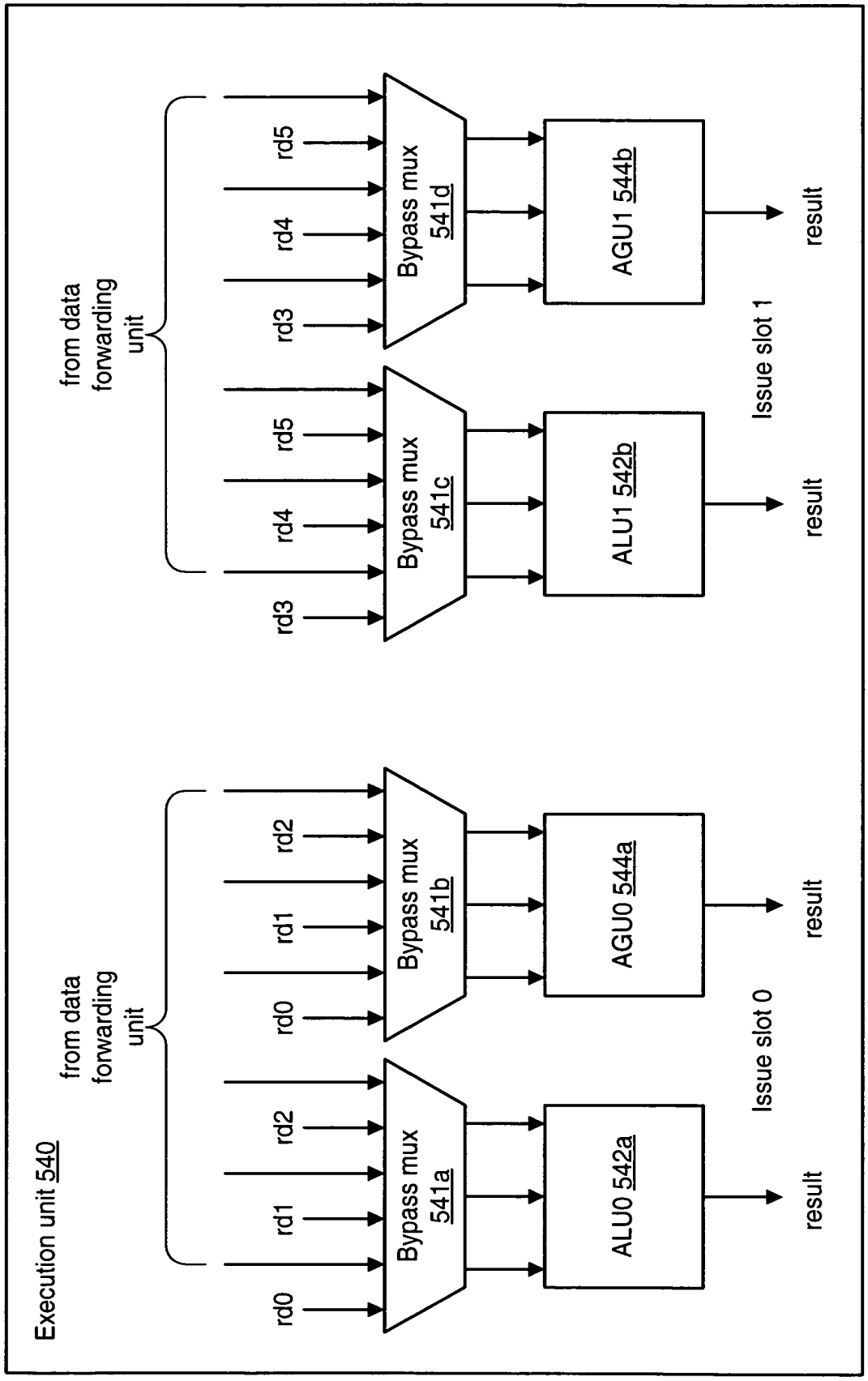
Execution unit 540
from data forwarding unit
rd0
rd1
rd2
Bypass mux 541a
ALU0 542a
result
rd0
rd1
rd2
Bypass mux 541b
AGU0 544a
result
Issue slot 0
from data forwarding unit
rd3
rd4
rd5
Bypass mux 541c
ALU1 542b
result
rd3
rd4
rd5
Bypass mux 541d
AGU1 544b
result
Issue slot 1

FIG. 5

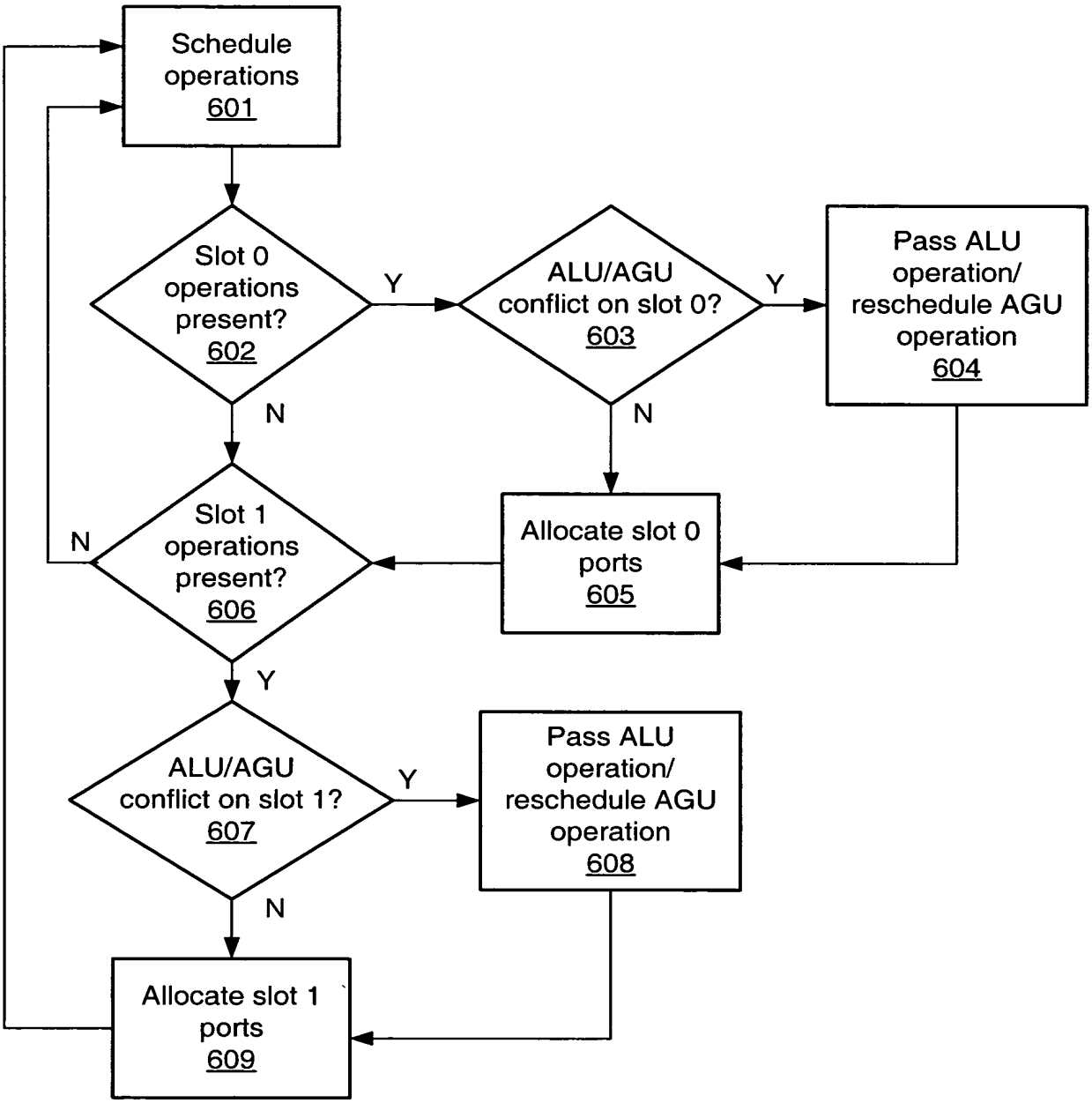
Schedule operations 601
Slot 0 operations present? 602
Y
ALU/AGU conflict on slot 0? 603
Y
Pass ALU operation/ reschedule AGU operation 604
N
N
Slot 1 operations present? 606
N
Allocate slot 0 ports 605
Y
ALU/AGU conflict on slot 1? 607
Y
Pass ALU operation/ reschedule AGU operation 608
N
Allocate slot 1 ports 609

FIG. 6

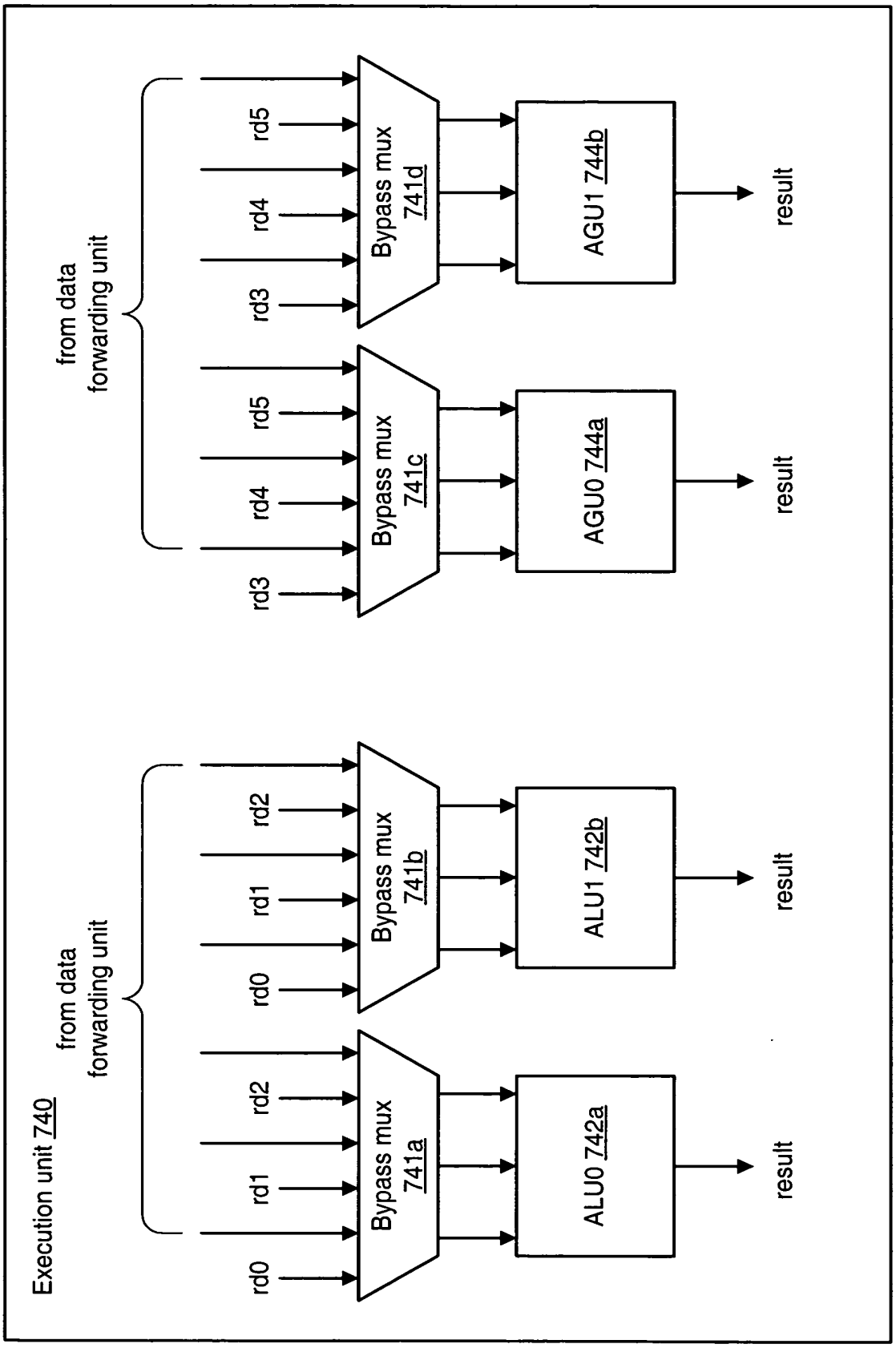
Execution unit 740
from data forwarding unit
rd0
rd1
rd2
Bypass mux 741a
ALU0 742a
result
rd0
rd1
rd2
Bypass mux 741b
ALU1 742b
result
from data forwarding unit
rd3
rd4
rd5
Bypass mux 741c
AGU0 744a
result
rd3
rd4
rd5
Bypass mux 741d
AGU1 744b
result

FIG. 7

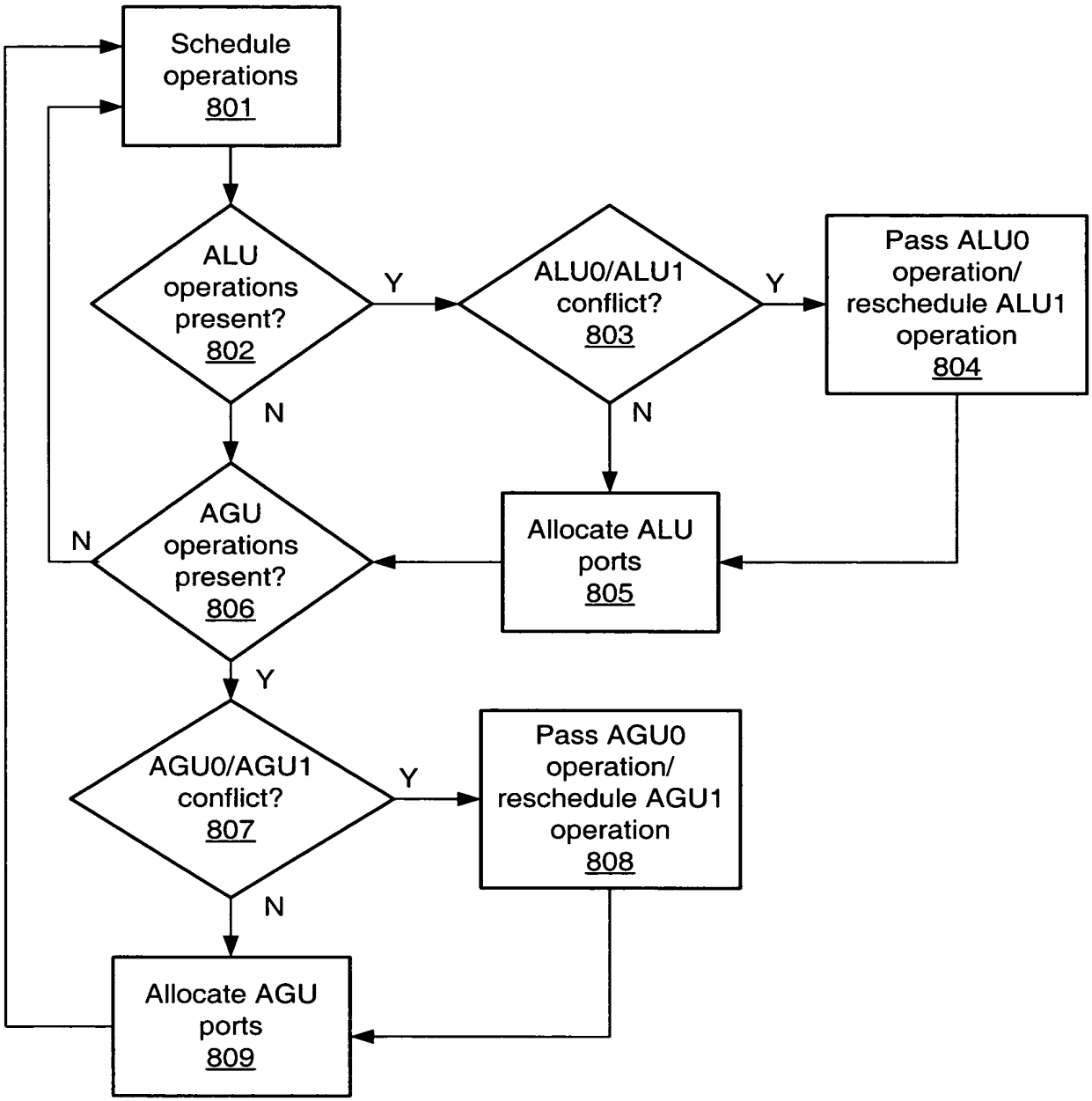
Schedule operations 801
ALU operations present? 802
Y
ALU0/ALU1 conflict? 803
Y
Pass ALU0 operation/ reschedule ALU1 operation 804
N
N
AGU operations present? 806
N
Allocate ALU ports 805
Y
AGU0/AGU1 conflict? 807
Y
Pass AGU0 operation/ reschedule AGU1 operation 808
N
Allocate AGU ports 809

FIG. 8

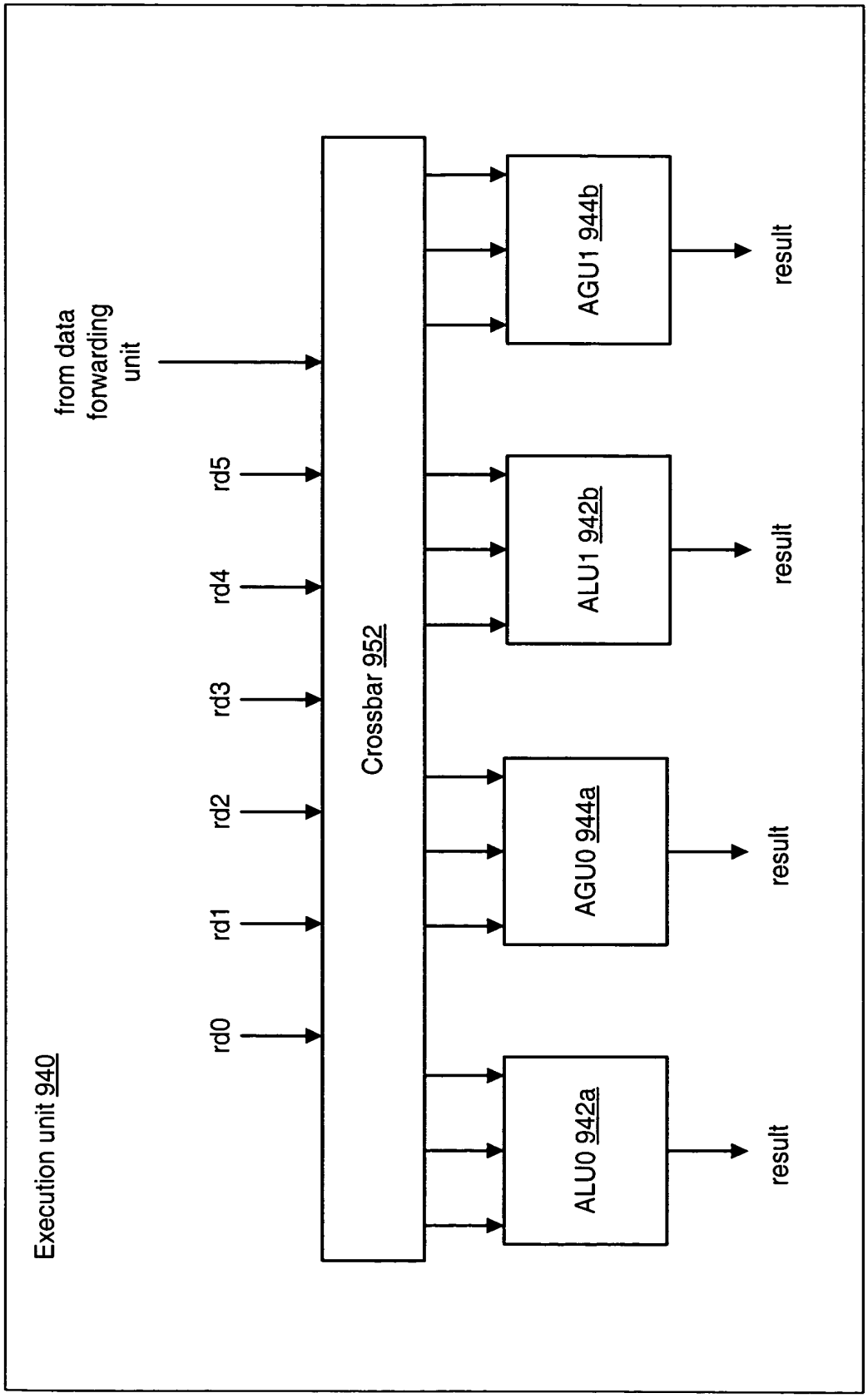
Execution unit 940
from data forwarding unit
rd0
rd1
rd2
rd3
rd4
rd5
Crossbar 952
ALU0 942a
AGU0 944a
ALU1 942b
AGU1 944b
result
result
result
result

FIG. 9

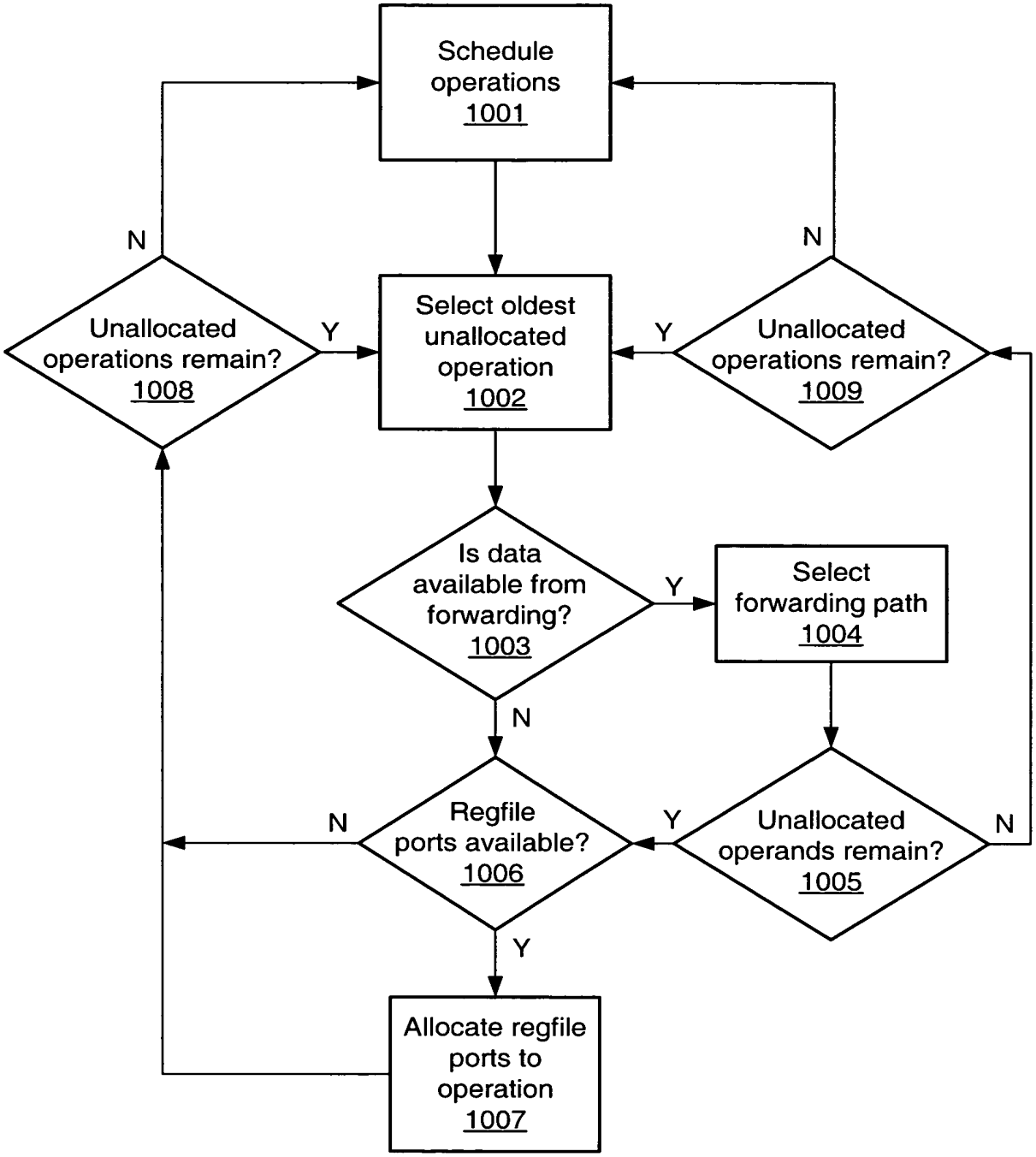
Schedule operations 1001
Unallocated operations remain? 1008
Y
N
Select oldest unallocated operation 1002
Y
N
Unallocated operations remain? 1009
Is data available from forwarding? 1003
Y
Select forwarding path 1004
N
Regfile ports available? 1006
N
Y
Unallocated operands remain? 1005
Y
N
Allocate regfile ports to operation 1007

FIG. 10